REMARKS

This paper is being provided in response to the Office Action mailed June 29, 2004, for the above-referenced application. In this response, Applicant has amended claims 1, 5, 6, 16 and 17 to clarify that which Applicant considers to be the invention. Further, Applicant has amended the title as requested in the Office Action. Applicant respectfully submits that the amendments to the claims are fully supported by the originally-filed specification and that the amendments to the title do not add new subject matter.

The objection to the drawings under 37 C.F.R. 1.83(a) is hereby traversed and reconsideration is respectfully requested. The Office Action indicates that the following feature of claim 1 is not illustrated in the figures: "each circuit string having an input terminal and an output terminal, in which an edge of a clock signal received at the input terminal proceeds in one direction and then is reversed in the proceeding direction thereof, based on a turn control signal generated on the basis of an edge of a clock signal next following the input clock signal, the clock edge proceeding in the direction reverse to the one direction, over a time equal to the time during which the clock edge proceeded in the one direction, so as to be output at the output terminal". Further, the Office Action indicates that the "comparing means" of claim 14 is not illustrated.

With respect to claim 1, Applicant directs general attention to Figures 1-5 of the present application illustrating one embodiment of the present invention and refers specifically, for example, to the description of circuit structure beginning on page 16, line 5 and circuit operation beginning on line 3, page 29 of the present application. Figure 1 illustrates two bidirectional

delay circuits strings 106 and 107 each having input and output terminals and Figure 5 is a timing chart illustrating circuit operation. The clock edge proceeding on the delay circuit string towards right has it proceeding direction reversed by the turn control signal generated, AFWD/ABWD (shown in Fig. 1), generated from the rising edge (R2) of the external clock signal (CLK), to proceed towards left to present itself at an output (BOA) of the delay circuit string (BDDA) 106. It is a basic characteristic of the delay circuit string of the BDD configuration that the time as from entering to the delay circuit strings 106 and 107 until turning around is equal to the time as from the turning around until outputting (indicated [tBDD] in Fig. 5). The edge output from the delay circuit string (BDDA) 106 reaches the output buffer (DOB) 109 through the post-delay circuit (POSTA) 112 and the multiplexer (MUX) 108 so that data is output at data output terminal (DQ). Applicant submits that the cited feature of claim 1 is adequately illustrated.

With respect to claim 14, Applicant directs attention to the lock mode decision circuit 320 shown in Figure 6 and described beginning on page 35, line 17 of the present application. The lock mode decision circuit is made up by a divide-by-2 frequency dividing circuit (DIV2) 321, receiving an output of the buffer circuit 301 as input, a second delay adding circuit (ADD2) 322 and a flip-flop 323, and performs the operation of switching the lock mode n to n=1 or n=2 depending on the frequency of the external clock signal (CLK). The lock mode decision circuit decides on the lock mode number based on a comparison of clock periods and delay times. (See, for example, page 39 lines 2-15 of the present application.) Applicant submits that the lock mode decision circuit provides adequate support for a "comparing means" recited in claim 14.

Applicant submits that all of the claimed features are adequately shown in the drawings. Accordingly, Applicant respectfully requests that the objections to the drawings be reconsidered and withdrawn.

The objection to the Title has been addressed by amendments contained herein. Accordingly, Applicant respectfully requests that this objection be reconsidered and withdrawn.

The objections to claims 6 and 16 for informalities have been addressed by amendments to the claims contained herein in accordance with the guidelines as set forth in the Office Action. Accordingly, Applicant respectfully requests that these objections be reconsidered and withdrawn.

The rejection of claims 1-20 under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement is hereby traversed and reconsideration is respectfully requested. Applicant refers to the above remarks concerning the objection to the figures with respect to the features of claim 1. As is noted above, the cited features of claim 1 are presented in detail in the specification and figures. Applicant submits that the features of claim 1 (and claim 17) are fully described and illustrated in such a way as to enable one of ordinary skill in the art to make and use the invention. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 17-20 under 35 U.S.C. 112, second paragraph, as being indefinite has been addressed by amendments contained herein in accordance with the guidelines set forth

in the Office Action. Accordingly, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 1-7, 10, 13, 15, 17 and 18 under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art Figure 9A and 9B (hereinafter "Applicant's APA") in view of U.S. Patent No. 6,359,480 to Isobe et al. (hereinafter "Isobe") and further in view of U.S. Patent No. 5,870,445 to Farwell (hereinafter "Farwell") is hereby traversed and reconsideration is respectfully requested.

Independent claim 1, as amended herein, recites a clock synchronization circuit. The circuit includes first and second bidirectional delay circuit strings, each circuit string having an input terminal and an output terminal. An edge of a clock signal received at the input terminal proceeds in one direction and then is reversed in the proceeding direction thereof, based on a turn control signal generated on the basis of an edge of a clock signal next following said input clock signal. The clock edge proceeding in the direction reverse to the one direction, over a time equal to the time during which the clock edge proceeded in the one direction so as to be output at the output terminal. First and second pre-stage delay circuits and first and second post-stage delay circuit, having delay times thereof being able to be variably set, are arranged at a pre-stage and a post-stage of the first and second bidirectional delay circuit strings, respectively. A multiplexing circuit receives output signals of the first and second post-stage delay circuits to output a multiplexed signal of the output signals. A delay time setting circuit variable controls the delay times of the first and second pre-stage delay circuits and the first and second post-stage delay circuits, wherein the delay time setting circuit variably controls the delay times of said pre-stage

and post-stage delay circuits according to a relationship between a minimum delay time for circuit operation and a period of said clock signal received by the clock synchronization circuit. The clock signal received by the clock synchronization circuit is supplied in common to the input terminals of the first and second pre-stage delay circuits. A phase controlling means alternately selects a first path including the first pre-stage delay circuit, the first bidirectional delay circuit string and the first post-stage delay circuit and a second path including the second pre-stage delay circuits, the second bidirectional delay circuit string and the second post-stage delay circuit, an interval of a preset cycle of the clock signal. Claims 2-15 depend directly or indirectly on independent claim 1.

Independent claim 17, as amended herein, recites a semiconductor device. The device includes a first buffer circuit having an input terminal for receiving a clock signal supplied to the semiconductor device and an output terminal for outputting the clock signal. A first delay circuit receives the clock signal output from the first buffer circuit, delays the clock signal by a preset time, and outputs the delayed signal. First and second pre-stage delay circuits, delay time thereof being able to be variably set, have input terminals connected in common to an output terminal of said first delay circuit and output a signal from said first delay circuit with delay. A phase selection circuit receives the clock signal output from the first buffer circuit to output first and second phase selection signals, activation of the first and second phase detection signals being switched in a controlled manner in an interval of one cycle of the clock signal. First and second bidirectional delay circuit strings are included, each circuit string having an input terminal and an output terminal. An edge of a clock signal received at the input terminal proceeds in one direction and then is reversed in the proceeding direction thereof, based on a turn control signal

generated on the basis of an edge of a clock signal next following the input clock signal. The clock edge proceeds in direction reverse to the one direction over time equal to the time during which the clock edge proceeds in the one direction so as to be output at the output terminal. A first control circuit receives the clock signal output from the first buffer circuit, the output signal of the first pre-stage delay circuit and the first phase selection signal to supply the output signal of the first pre-stage delay circuit to an input terminal of the first bidirectional delay circuit as well as to output a turn control signal, based on the clock signal output from the first buffer circuit, when the first phase signal is activated. A second control circuit receives the clock signal output from the first buffer circuit, the output signal of the second pre-stage delay circuit and the second phase selection signal to supply the output signal of the second pre-stage delay circuit to an input terminal of the second bidirectional delay circuit as well as to output a turn control signal, based on the clock signal output from the first buffer circuit, when the second phase signal is activated. First and second post-stage delay circuits, delay time thereof being able to be variably set, are arranged at a post-stage of said first and second bidirectional delay circuit strings, respectively. A multiplexing circuit receives output signals of said first and second post-stage delay circuits to output a multiplexed signal of said output signals of said first and second post-stage delay circuits. An output circuit outputs data at a data output terminal based on the output signals of said multiplexing circuit. A delay time setting circuit for variably setting the delay time of said first and second pre-stage delay circuits and the delay time of said first and second post-stage delay circuits, depending on the period of said clock signal and the delay time of said first delay circuit. The delay time of said first delay circuit is equal to the sum of the delay time of said first buffer circuit, the delay time of said multiplexing circuit and the delay time of said output circuit. Switching is made between a first path including said first pre-stage

delay circuit, said first bi-directional delay circuit string and said first post-stage delay circuit string and a second path including said second pre-stage delay circuit, said second bi-directional delay circuit string and said second post-stage delay circuit, in an interval of a preset cycle of said clock signal. A signal synchronized with the edge of said clock signal is output from said data output terminal. Claims 18-20 depend directly or indirectly on independent claim 17.

Applicant's APA, Figures 9A and 9B, show an arrangement and timing chart of a conventional clock synchronization signal including bidirectional delay circuit strings.

The Isobe reference discloses a synchronizing circuit for generating a signal synchronizing with a clock signal. The circuit includes a delay monitor 13 that receives the output of a buffer circuit 12 and supplies an output signal to a first delay line 14. An output buffer circuit 17 is connected to the output terminal of a second delay line 16. (See Figure 1 and col. 4, line 48 to col. 5, line 14 of Isobe.)

The Farwell reference discloses a frequency independent clock synchronizer. The Office Action cites Farwell as disclosing a delay circuit having delay times variably set by a shift register 51. (See Figure 4 and col. 3, lines 16-61 of Farwell.)

Applicant's independent claims, as amended herein, recite that a clock synchronizing circuit or semiconductor device includes bidirectional circuit strings, pre and post-stage delay circuits and *a delay time setting circuit for performing control for variably setting the delay time of said first and second pre-stage delay circuits and the delay time of said first and second post-*

stage delay circuits, wherein said delay time setting circuit variably controls the delay times of said pre-stage and post-stage delay circuits according to a relationship between a minimum delay time for circuit operation and a period of said clock signal received by the clock synchronization circuit, or where the delay time setting circuit controls delay times *dependent on a period of the clock signal and the delay time of a first delay circuit.* Applicant has found that a clock synchronization circuit having pre and post-stage delay circuits with delay times variably controlled by a delay time setting circuit according to the relationship as recited helps ensure that consecutive operating periods do not overlap with one another and provides for a short minimum operating period that can be realized with small area and low power consumption. (See, for example, page 17, line 11 to page 18, line 7 of the present application.)

Applicant respectfully submits that the prior art of record, taken alone or in combination, does not teach or fairly suggest at least the above noted features as claimed by Applicant. Specifically, Applicant's APA does not show pre and post-stage delay circuits connected, respectively, to bidirectional delay circuit strings and does not disclose a delay time setting circuit that variably controls delay. The Office Action cites Isobe as disclosing pre and post-stage delay circuits 13 and 17 (Isobe's Figure 1) and cites Farwell as disclosing a variable delay controlling unit, shown as a shift register 51 (Farwell's Figure 3). Applicant respectfully submits that Isobe does not disclose variably controlling delay times, and consequently provides no basis for variable control of pre and post stage delay circuits that would be performed according to a particular relationship, such as that recited Applicant.

Specifically, the Office Action asserts that elements 12(D1), 13(D1, D2) and 17(D2) disclosed in Fig. 1 of Isobe would correspond to the pre-stage delay and the post-stage delay, as recited in the present claimed invention. However, according to Isobe's specification, 12 is an input buffer, 17 is an output buffer, and 13 is a replica delay (termed "delay monitor 13" in Isobe). The input buffer and output buffer are mere buffer circuits which are never used to positively delay the signal, nor to provide a variable delay time. The replica delay is dedicated to make its output delay equal to the sum of the delay time of the input buffer and that of output buffer, thus resulting in no variable delay time at all. Accordingly, there is arguably nothing in Isobe that would suggest any variable delay of delay monitor 13 and, furthermore, the delay of delay monitor 13 is necessarily dependent on the delay of the first and second buffer circuits and is not controlled according to the relationships as recited in the present claimed invention. To help clarify this point and for purposes of example only, Applicant refers to Fig. 1 of the present specification in which Applicant illustrates an input buffer as CLKB, an output buffer as MUX and DOB and a replica delay as REP but then further illustrates the feature of variable delay times by elements of variable delay PREA/B and POSTA/B.

Applicant respectfully submits that Farwell fails to overcome the above-noted deficiencies of the Isobe reference with respect to Applicant's present claimed invention. Farwell discloses a variable delay unit that is a shift register 51. However, Farwell does not disclose any post-stage delay circuits and does not disclose control of pre and post-stage delay circuits according to the relationships as recited by Applicant. Further, Applicant respectfully submits that Isobe does not arguably provide for a circuit that can utilize variable delay and, in fact, *teaches away* from variable delay by the structure of Isobe's delay monitor 13 that is simply a

sum of delay times of the input and output buffers. Thus, Applicant submits that it is not proper to combine the shift register of Farwell with Isobe in an attempt to teach variable delay in Isobe's circuit.

Accordingly, Applicant respectfully submits that neither Applicant's APA, Isobe, nor Farwell, taken alone or in any combination, teaches or fairly suggests at least the features of a clock synchronizing circuit or semiconductor device includes bidirectional circuit strings, pre and post-stage delay circuits and *a delay time setting circuit for performing control for variably setting the delay time of said first and second pre-stage delay circuits and the delay time of said first and second post-stage delay circuits, wherein said delay time setting circuit variably controls the delay times of said pre-stage and post-stage delay circuits according to a relationship between a minimum delay time for circuit operation and a period of said clock signal received by the clock synchronization circuit*, or where the delay time setting circuit controls delay times *dependent on a period of the clock signal and the delay time of a first delay circuit*, as is claimed by Applicant. In view of the above, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

With respect to claims 8, 9, 11, 12, 14, 16, 19 and 20, in view of the above remarks concerning the adequate enablement of all claimed features, Applicant respectfully requests that these claims be appropriately considered and examined. Applicant notes that claim 16 has been rewritten into independent form.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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